SST Technical Note

Differences Between SST-PFB3-PCI and 5136-PFB-PCI

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This document applies to the SST-PFB3-PCI and 5136-PFB-PCI interface cards.

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Preface

Preface sections:

- Purpose of this technical note
- Conventions

Purpose of this Technical Note

This technical note describes the functional differences between the 5136-PFB-PCI and the SST-PFB3-PCI Profibus interface cards. It also describes any differences between the Win32 API for the two cards.

Note

Each module has an accompanying manual that describes its operation. Refer to the applicable manual for firmware-specific information.

Conventions

This technical note uses stylistic conventions, special terms, and special notation to help enhance your understanding.

Style

The following stylistic conventions are used throughout this technical note:

Bold	indicates field names, tab names, and options or selections
Italics	indicates a command or dialog box
CAPS	indicates a button that the user may press or specific key selection, such as ENTER, TAB, CTRL, ALT, DELETE
`Code Font`	indicates command line entries or text that you'd type into a field
Underlining	indicates a hyperlink
">" delimiter	indicates how to navigate through a hierarchy of menu selections/options

Special Terms

The following special terms are used throughout this technical note:

Card	the SST-PFB3-PCI interface card
Firmware	the software running on the card
Module	a synonym for *firmware*

Special Notation

The following special notations are used throughout this technical note:

Warning

Warning messages alert the reader to situations where personal injury may result. Warnings are accompanied by the symbol shown, and precede the topic to which they refer.

Caution

Caution messages alert the reader to situations where equipment damage may result. Cautions are accompanied by the symbol shown, and precede the topic to which they refer.

Note

A note provides additional information, emphasizes a point, or gives a tip for easier operation. Notes are accompanied by the symbol shown, and follow the text to which they refer.

Contents

1
Introduction

Chapter sections:

- Card overview
- Reference documents

1.1 Card Overview

The SST-PBF3-PCI is the next Generation Profibus PCI card. When possible, backward compatibility is maintained with the legacy 5136-PFB-PCI, but the new SST-PFB3-PCI is not a drop in replacement for the existing 5136-PFB-PCI card.

The 5136-PFB-ISAand the SST-PFB3-PCI card can:

- Act as a DP slave
- Act as a DP master
- Send and receive FDL (layer 2) messages
- Support Master Class 2
- Support simultaneous operation in all of the above modes
- Support the standard Profibus baud rates of 9.6K, 19.2K, 93.75K, 187.5K, 500K, 750K, 1.5M, 3M, 6M and 12M baud.

Note

The SST-PFB3-PCI does not support FMS messaging.

While control of the legacy 5136-PFB-PCI card (for example, interrupts and reset) was handled by writing to the PCI configuration space (Section 2.4), this is no longer the case with the new SST-PFB3-PCI.

The SST-PFB3-PCI card is controlled through a separately mapped PCI memory area. This memory area is also used to access new features, like the ability to read the LED status (Section 2.2). The PCI configuration space of the new design does not normally need to be written to by the host application; it is normally only used by the host system drivers to determine where card resources have been allocated in the host system.

1.2 PCI Compatibility

1.2.1 Overview

Table 1: PCI Compatibility Table

PCI Revision	Supply Voltage Provided by Motherboard		PCI I/O signaling voltage level of Motherboard	
	3.3V	5V	3.3V	5V
2.1	[1]Optional	Mandatory	Not supported	Supported
2.2	Mandatory	Mandatory	Supported	Supported
2.3	Mandatory	Mandatory	Supported	Not supported
SST Product				
SST-PFB3-PCI	Required	Required	[2]Supported	[2]Supported
5136-PFB-PCI	Not Required	Required	[3]Not Supported	Supported

1) The SST-PFB3-PCI requires both 3.3V and 5V to be supplied by the motherboard. Because 3.3V supply voltage is optional in PCI revision 2.1, the SST-PFB3-PCI may not function in some PCI 2.1-compliant motherboards.

2) The SST-PFB3-PCI will auto detect the motherboard PCI I/O signaling level and adjust its signaling level accordingly, allowing it to function in PCI systems that support either 5V or 3.3V I/O signaling levels.

3) The 5136-PFB-PCI does not support 3.3V motherboard signaling levels. Because of this, the 5136-PFB-PCI is not PCI 2.3-compliant.

1.2.2 Summary

SST-PFB3-PCI:

- PCI 2.2-compliant
- Will operate in PCI 2.2- and 2.3-compliant systems
- Will also operate in PCI 2.1-compliant systems that have implemented the optional 3.3V supply voltage

5136-PFB-PCI:

- PCI 2.1-compliant
- Will operate in PCI 2.1- and 2.2-compliant systems

1.3 Reference Documents

For information on ProfiBus, refer to one of the following:

- ProfiBus standard DIN 19 245 parts 1, 2 and 3. Part 1 describes the low-level protocol and electrical characteristics, Part 2 describes FMS, and Part 3 describes DP.

- European Standard EN 50170

2
Host Interface

Chapter sections:

- SST-PFB3-PCI configuration space
- SST-PFB3-PCI host register definitions
- Loading the SST-PFB3-PCI
- 5136-PFB-PCI configuration space
- 5136-PFB-PCI host register definitions
- Loading the 5136-PFB-PCI
- Profibus host memory interface

2.1 SST-PFB3-PCI Configuration Space

Table 2: PCI Configuration Space Table

PCI CFG Register Address	Register Function 32 24 23 16 15 8 7 0				PCI Writable
0x00	Device ID 0x0033			Vendor ID 0x133D	N
0x04	Status			Command	Y
0x08	Class Code			Revision ID	N
0x0C	BIST	Header ID	PCI Latency	CacheLineSize	Y[7:0]
0x10	PCI Base Address 0 Memory, 128 bytes, Reserved				Y
0x14	PCI Base Address 1 Not Used				Y
0x18	PCI Base Address 2 Memory, 256K bytes Profibus Interface See section 2.7				Y
0x1C	PCI Base Address 3 Memory, Host Interface Registers See section 2.2				Y
0x20	PCI Base Address 4 Not Used				Y
0x24	PCI Base Address 5 Not Used				Y
0x28	Cardbus CIS Pointer (Not supported)				N
0x2C	Subsystem Device ID 0x9030			Subsystem Vendor ID 0x10B5	N
0x30	PCI Base Address for Local Expansion ROM				Y
0x34	Reserved				N
0x38	Reserved				N
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]

Note

Refer to the PCI specification and your particular OS documentation for the function of all other PCI configuration space registers and their typical uses.

Note

Typically, the PCI configuration space registers do not need to be written to by the host system driver. A plug and play BIOS and/or host operating system will ensure there are no resource conflicts in the system.

2.2 SST-PFB3-PCI Host Register Definitions

The SST-PFB3-PCI host registers are mapped into a separate region of PCI memory space (PCI Region 3). The base address of where this region is mapped in the host system can be found by reading the PCI configuration space at offset 0x1C. See section 2.1 for PCI configuration space information.

Register definitions are as follows.

Table 3: Host Register Layout

Offset	Name	7	6	5	4	3	2	1	0
00h	Control	CardRun (r/w)	MemEn (r/w)	IntEn (r/w)	WdTout (read)	HostIrq1 (r/w)	HostIrq0 (r/w)	CardIrq1 (r/w)	CardIrq0 (r/w)
01h	AddrMatch	1	AM18	AM17	AM16	AM15	AM14	X	X
02h	BankSelect	0	0	0	BA16	BA15	BA14	X	X
03h	WinSize	WS19	WS18	WS17	WS16	WS15	WS14	WS13	WS12
04h	HostIrq (r/w)	X	X	X	X	IrqLevel			
05h	LedReg (read)	X	X	X	X	CommRed	CommGrn	SYSRed	SYSGrn
06h	Debug (r/w)	HWReset	X	X	JTAGEN	CPUTRST	CPUTMS	CPUTDI	CPUTCK
07h	HDR	HostDataReg (written by CPU)							
08h – 1Fh	Reserved								

2.2.1 Control Register

Table 4: Control Register Bit Descriptions

Bit Name	Description
CardRun	High (1) indicates that the card is in “Run” mode (CPU is out of reset and will attempt to execute firmware). Low (0) indicates that the card is in “Stop” mode (CPU is in reset) or a WdTout has occurred (also see WdTout bit).
MemEn	High (1) enables shared memory decoding of addresses in this board’s range. This board’s range is defined by the AddrMatch register.
IntEn	High (1) enables interrupts on IrqLevel when a HostIrq bit is high (1).
WdTout	High (‘1’) indicates that a watchdog timeout has occurred.
HostIrq1, HostIrq0, CardIrq1, CardIrq0	• High (‘1’) indicates that the specified interrupt is in progress, and has not yet been serviced • Writing HostIrq1, HostIrq0 high (‘1’) cause the pending Host interrupt to end (done by Interrupt service routine running on the host) • Writing CardIrq1, CardIrq0 high (‘1’) generate an interrupt to the card at the appropriate level

2.2.2 AddrMatch Register

Bit Name	Description
AM18-AM14	Reserved. This register always reads zero, and writing these bits has no effect.

2.2.3 BankSelect Register

Bit Name	Description
BA16-BA14	Reserved. This register always reads zero, and writing these bits has no effect.

2.2.4 WinSize Register

Bit Name	Description
Winsize	Reserved. This register always reads 0x3F, and writing this register has no effect.

2.2.5 HostIrq Register

Bit Name	Description
IrqLevel	Reserved. This register always reads zero, and writing this register has no effect.

2.2.6 LedReg Register

The LedReg register represents the state of the card LEDs. The state of this register is controlled by firmware. Reading the register will reflect the following LED states:

Table 5: System LED

The System LED conforms to the following standard.

SysGrn	SysRed	LED Colour
0	0	Off
0	1	Red
1	0	Green
1	1	Amber

Table 6: Communication LED

The Communication LED conforms to the following standard.

CommGrn	CommRed	LED Colour
0	0	Off
0	1	Red
1	0	Green
1	1	Amber

2.2.7 Debug Register

Reserved for future use.

2.2.8 HDR Register

Reserved for future use.

2.3 Loading the SST-PFB3-PCI

To load and start the firmware module, follow these steps:

1. Write the contents of the entire firmware file into shared memory, starting at offset zero (0).
2. If your application requires interrupts from the card, bit-wise OR the value 0x20 (IntEn) to the Control register.
3. Bit-wise OR the value 0x80 (CardRun) to the Control register to start the firmware module.
4. Start a 2 second timeout timer.
5. Wait for bit 0 (HostIrq0) in the Control register to set, or for the timer to expire.
6. If the timer has expired, the firmware module failed to start. Write zero to the Control register to place the card into a Reset. If this problem persists, contact technical support for assistance.
7. Check for the appropriate success indication, as per the firmware manual.

2.4 5136-PFB-PCI Configuration Space

The 5136-PFB-PCI card has two PCI devices:

- Function 0: Primary PCI to PCI bridge that is not used by the card for any ProfiBus-related functions
- Function 1: Secondary PCI to i960 local ram bridge (ATU) that is the primary shared RAM interface to the card.

Function 0 and Function 1 are described in the following two tables.

Table 7: Function 0

Bridge Configuration Header				PCI Config Addr Offset	
Device ID		Vendor ID		00h	PCI to PCI Bridge
Primary Status		Primary Command		04h	
Class Code			Revision ID	08h	
Reserved	Header Type	Primary Latency Timer	Cacheline Size	0Ch	
Reserved				10h 14h	
Secondary Latency Timer	Subordinate Bus number	Secondary Bus number	Primary Bus number	18h	
Secondary Status		I/O Limit	I/O Base	1Ch	
Memory Limit		Memory Base		20h	
Prefetchable Memory Limit		Prefetchable Memory Base		24h	
Reserved				28h 2Ch 30h	
Bridge subsystem ID		Bridge subsystem Vendor ID		34h	
Reserved				38h	
Bridge Control		Reserved		3Ch	
Secondary IDSEL Select		Extended Bridge Control		40h	i960®RX I/O Processor Specification
Primary Bridge Interrupt Status				44h	
Secondary Bridge Interrupt Status				48h	
Secondary Arbitration Control				4Ch	
PCI Interrupt Routing Select				50h	
Reserved		Secondary I/O Limit	Secondary I/O Base	54h	
Secondary Memory Limit		Secondary Memory Base		58h	
Reserved		Secondary Decode Enable		5Ch	

Table 8: Function 1

ATU Configuration Space Header				PCI Config Addr Offset
ATU Device ID		ATU Vendor ID		00h
Primary ATU Status		Primary ATU Command		04h
ATU Class Code			ATU Revision ID	08h
ATU Bist	ATU Header Type	ATU Latency Timer	ATU Cacheline Size	0Ch
Primary Inbound ATU Base Address				10h
Reserved				14h 18h 1Ch 20h 24h 28h
ATU Subsystem ID		ATU Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved				34h 38h
ATU Max. Latency	ATU Min. Grant	ATU Interrupt Pin	ATU Interrupt Line	3Ch

Table 9: 5136-PFB-PCI Configuration Space Table

Register Name	Function #	Value	Description	PCI Configuration Space Address
Vendor ID	0	0x8086	Intel Vendor ID	0x00 (PCI reg 0x00)
Device ID	0	0x0960	Intel Device ID for I960RP	0x00 (PCI reg 0x00)
Extended Control Bridge	0	Bit 5 – reset I960	Set bit 5 to reset the I960. When the reset is finished, the bit is cleared by the 5136-PFB-PCI	0x40 (PCI reg 0x10)
Vendor ID	1	0x133D	SST Vendor ID	0x00 (PCI reg 0x00)
Device ID	1	0x1000	SST Device ID	0x00 (PCI reg 0x00)
Primary Inbound ATU Base Address	1	Set by PNP BIOS	The base address that the card occupies in memory	0x04 (PCI reg 0x01)
ATU Interrupt Line	1	Set by PNP BIOS	The PC Interrupt controller mapped IRQ line (3-15)	0x3C (PCI reg 0x0F)

2.5 5136-PFB-PCI Host Register Definitions

Unlike the SST-PFB3-PCI card, the 5136-PFB-PCI card does not contain Host Registers. The card is controlled through the PCI configuration space and the Profibus Interface. See section 2.7 for a description of the Profibus Interface area, and section 2.4 for information on the 5136-PFB-PCI PCI configuration space registers.

2.6 Loading the 5136-PFB-PCI

1. Follow these steps to load the 5136-PFB-PCI:
2. Read the Primary Inbound ATU Base Address at PCI register 4, function1, and save this value for later use.
3. Read the ATU Interrupt Line Register from register 0Fh of function1 and save this value for later use. The interrupt line value is the least significant byte of this register.
4. Reset the i960 by using bit 5 of the Extended Bridge Control Register (10h of function 0). Wait for i960 to come up.
5. Restore the saved values from steps 1 and 2 to the primary inbound ATU Base Address register and ATU Interrupt Line Register, respectively.
6. Enable the 5136-PFB-PCI card memory space by setting bit 1 (02h) of the Primary ATU Command Register (function1, register 1). Wait for the boot code to start by monitoring the byte location at base address + 1FFFFFh for the value BAh.
7. Load the card module (pcipfrofi.ss1) to memory starting at base address +1000h.
8. Write a 01 to base address +1FFFFFh to tell the boot code to run the firmware.
9. Wait for the firmware start up to complete by monitoring the base address +1FFFFF for the value 5Ah. The firmware copyright message and version string will be present at base address 1FFF00Hh.
10. Clear the byte at base address +1FFFFFHh to allow the firmware to continue.
11. Wait for the pfbCommand Register (base address + 8000h) to be set to E0h.
12. The implementation of PNP BIOS is defined by the PCI SIG. Please refer to the PCI Local Bus Specification Rev 2.1 and PCI BIOS Specification Rev 2.1. The latter document will define how to access the PCI configuration space of the 5136-PFB-PCI card.

2.7 Profibus Host Memory Interface

Both the 5136-PFB-PCI and the SST-PFB3-PCI cards use a common Profibus interface. The Profibus interface is logically divided into 16K byte pages. All pages are mapped into the host system memory space contiguously.

Note

Refer to the software manuals for 5136-PFB-PCI and SST-PFB3-PCI Interface details..

3
Win32 API

Chapter sections:

- API differences

3.1 API Differences

No new API calls will be added to the existing API set for the SST-PFB3-PCI; however, some of the existing calls will have new extensions.

Note

The API extensions will not affect legacy applications written for the old Win32 API. Application written for the old API will be forward compatible with the new API.

- PFB_WriteHC and PBB_ReadHC will have added “Signal parameter” extensions
- Refer to the “Win32 API for Profibus Interface Cards” manual for details on the PFB_WriteHC and PFB_ReadHC API calls
- Refer to the “Signal ID” table in the following section for details on the additions to the “Signal parameter” extension added to the API for the SST-PFB3-PCI card

3.1.1 PFB_WriteHC and PFB_ReadHC Signal ID Extensions

Table 10: Signal ID Extensions

Signal ID	Name	Access	Description	Supported Hardware Platforms
0	BCR_OFS	R/W	Board Control Register See 5136-PFB-PCI hardware users guide for register details.	Neither
1	MCR_OFS	R/W	Memory Control Register See 5136-PFB-PCI hardware users guide for register details.	Neither
2	MPR_OFS	R/W	Memory Page Register See 5136-PFB-PCI hardware users guide for register details.	5136-PFB-PCI SST-PFB3-PCI
3	ICR_OFS	R/W	Interrupt Control Register See 5136-PFB-PCI hardware users guide for register details.	Neither
4	PFB3_CTRL_OFS	R/W	Control Register See Register Description below for details.	SST-PFB3-PCI
5	PFB3_ADDR_OFS	R	AddrMatch Register	SST-PFB3-PCI

Signal ID	Name	Access	Description	Supported Hardware Platforms
			See Register Description below for details.	
6	PFB3_BANK_OFS	R	BankSelect Register See Register Description below for details.	SST-PFB3-PCI
7	PFB3_WINSIZE_OFS	R	WinSize Register See Register Description below for details.	SST-PFB3-PCI
8	PFB3_HOSTIRQ_OFS	R	HostIrq Register See Register Description below for details.	SST-PFB3-PCI
9	PFB3_LED_OFS	R	LedReg Register See Register Description below for details.	SST-PFB3-PCI
10	PFB3_DEBUG_OFS	R/W	Debug Register See Register Description below for details.	SST-PFB3-PCI
11	PFB3_HDR_OFS	R/W	HDR Register See Register Description below for details.	SST-PFB3-PCI
12-255	Reserved			

Refer to section 2.2 for hardware register definitions.

4

Profibus Connectors

Chapter sections:

- Connector differences

4.1 Connector Differences

The 5136-PFB-PCI card has both a Combicon and a D-sub9 connector, whereas the SST-PFB3-PCI only contains a D-sub9 connector. For additional details, refer to each card's hardware manual.

A

Technical Data

Appendix sections:

- SST-PFB3-PCI technical data
- 5136-PFB-PCI technical data

A.1 SST-PFB3-PCI Technical Data

Table 11: SST-PFB3-PCI Technical Data

Part Number	SST-PFB3-PCI
Function	Single channel Profibus Master/Slave, PCI 2.2- and PCI 2.3-compliant
Current Consumed	Estimated Max 300mA @5V, 450mA @3V
Environmental	Operating Temperature of 0 – 60 degrees Celsius
Card Connector	Standard Profibus DB-9 connector

A.2 5136-PFB-PCI Technical Data

Table 12: 5136-PFB-PCI Technical Data

Part Number	5136-PFB-PCI
Function	Single channel Profibus Master/Slave, PCI 2.1
Current Consumed	Max 750mA @5V
Environmental	Operating Temperature of 0 – 50 degrees Celsius
Card Connector	Standard Profibus DB-9 connector, Phoenix Combicon connector

B

Technical Support

Appendix sections:

- Technical support

B.1 Technical Support

Technical support is available during regular business hours, Eastern Time, by telephone, fax, email, or from www.mySST.com.

Note

Documentation, software updates, and other technical notes are also available on our website.

North America

Canada:
Tel: 519-725-5136
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